Amendments to the Specification:

In paragraph [0014]:

The key cells 60, 61 within the key module 52 include switches SW_{60}, SW_{61} respectively. The output end OUT_{60} of the key cell 60 (as well as the output end OUT_{61} of the key cell 61) is electrically connected to either a first voltage Vcc or a second voltage GND according to the opening and closing of the switch SW_{60}. That is, when the key cell 60 is pressed, the switch SW_{60} is ~~turned off~~ closed and the output end OUT_{60} is electrically connected to the second voltage GND so that a logic low voltage V_L is output. On the contrary, when the key cell 60 is released, the switch SW_{60} is ~~turned on~~ opened and the output end OUT_{60} is electrically connected to the first voltage Vcc so that a logic high voltage V_H is output. The logic high signal and the logic low signal on the output ends OUT_{60}, OUT_{61} form the input signals to the parallel-to-serial register 56.

In paragraph [0015]:

The detect circuit 54 includes one capacitor corresponding to each key cell within the key module 52 (as shown by capacitors 64, 65 corresponding to the key cells 60, 61 respectively within the key module 52 in Fig.2). An amplifier 66 is electrically connected to the capacitors 64, 65 for amplifying the voltage in the capacitors 64, 65. Two comparators 68, 70 are electrically connected to the amplifier 66 for comparing the voltage output by the amplifier 66 and outputting the control signal when the voltage output from the output end OUT_{amp} of the amplifier 66 is in a predetermined range. Finally, an OR gate 72 is electrically connected to the comparator 68, 70.

In paragraph [0016]:

At the moment when the key cell 60 (similar for key cell 61 or any other key cell) within the key module 52 is pressed or released, the switch SW_{60} of the key cell 60 is

accordingly ~~switched off~~ closed (or switched on) or ~~switched on~~ opened (or switched off), and the output end OUT_{60} is accordingly electrically connected to the second voltage GND or the first voltage Vcc. In this situation, the detect circuit 54 detects a transient voltage V_{ts} of 100-150mV formed in the capacitor 64 (or the capacitor 65). Please refer to Fig.3 showing a waveform diagram of the transient voltage V_{ts} and the control signal CS in the capacitors 64, 65 detected by the detect circuit 54 whenever the key cells 60, 61 within the key module 52 of the key board 50 are pressed or released. As shown in Fig.3, at the moment when the key cell 60 (similar for key cell 61) is pressed at time t_1 (or t_2), the switch SW_{60} of the key cell 60 is ~~switched off~~ closed, and the output end OUT_{60} of the key cell 60 is connected to the second voltage GND (i.e. the input signal on the output end OUT_{60} of the key cell 60 becomes a logic low voltage V_L). In this situation, the detect circuit 54 detects a negative transient voltage V_{ts-} in the capacitor 64. On the other hand, at the moment when the key cell 60 (similar for key cell 61) is ~~pressed~~ released at time t_3 (or t_4), the switch SW_{60} of the key cell 60 is ~~switched on~~ opened, and the output end OUT_{60} of the key cell 60 is connected to the first voltage Vcc (i.e. the input signal on the output end OUT_{60} of the key cell 60 becomes a logic high voltage V_H). In this situation, the detect circuit 54 detects a positive transient voltage V_{ts+} in the capacitor 64. The amplifier 66 amplifies the positive transient voltage V_{ts+} and the negative transient voltage V_{ts-} and outputs the amplified positive transient voltage V_{ts++} and the amplified negative transient voltage V_{ts--} into an input end of the comparators 68, 70. In the present invention, the comparators 68, 70 are divided into a positive comparator 68 and a negative comparator 70. The detect circuit 54 outputs the control signal CS from an output end OUT_{or} of the OR gate 72 either when ~~either~~ the amplified positive transient voltage V_{ts++} exceeds a positive reference voltage V_{ref+} on the other input end of the positive comparator 68, or when the amplified negative transient voltage V_{ts--} is lower than a negative reference voltage V_{ref-} on the other input end of the negative comparator 70.